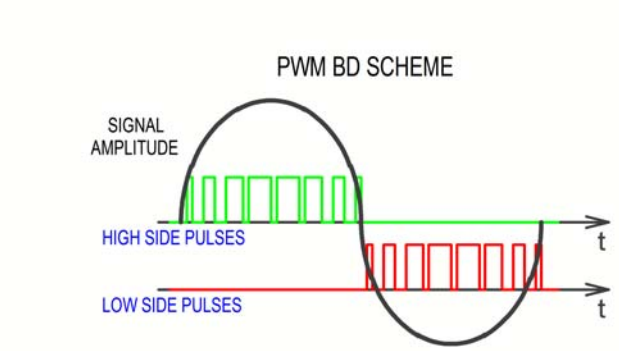
THE SWITCHINGLOW PROJECT REVISITED
USB PWM MODULATOR

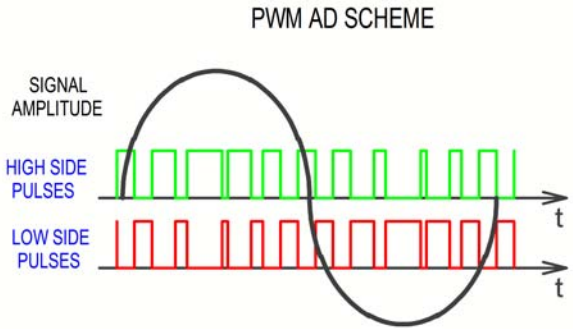
The **SWTGLW USB MOD** is a full digital, USB audio input, stereo PWM type BD modulator based on the USB-I2S bridge PCM2706C and an LCMXO2-1200HC-6SG32C FPGA programmed with a proprietary algorithm running at its 400MHz maximum clock speed.

This USB powered board converts 48KHz sample rate, 16 bit stereo audio streaming carried by an USB 2.0 FS Audio Class 1.1 connection in four 192KHz width modulated pulses streams according to a *type BD PWM* scheme:

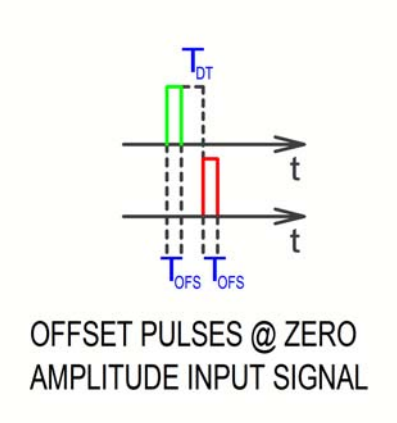
- zero audio signal = 0% duty cycle on both LOW and HIGH side output
- positive audio signal = proportional duty cycle on HIGH side output only
- negative audio signal = proportional duty cycle on LOW side output only



This allows high efficiency, zero *idle current* and EMI reduction at the power bridge circuit, as each side of it switches only during the positive or the negative part of the input suignal while the other side remains in the off state.
In a classic *type AD PWM* scheme the power bridge circuit is switched by a PWM signal with 50% duty cycle at zero audio amplitude, a proportional duty cycle > 50% when the audio signal is positive and a duty cycle < 50% when the audio signal is negative; this means the power bridge circuit is always switching with a large duty cycle even if the audio signal is zero, leading to the *idle current.* Further both the two sides of the power bridge circuits are always switching regardless the polarity of the audio signal, leading to a twice amount of EMI compared to the *type BD* PWM.



In the *type AD PWM* every small variation of the duty cycle around the zero amplitude 50% duty cycle becames a small low level audio signal at the output of the power bridge circuit.
With the *type BD PWM* in case of very low amplitude audio signal, very narrow pulses can be generated at the PWM outputs; if the power devices used in the power bridge circuit are not enough fast, these short pulses will be not transefered to the loudspeakers resulting in a noisy distortion occuring at the lower audio levels.
To avoid this drawback, the **SWTGLW USB MOD** circuit provides a sort of ***offset pulses***: at zero audio signal the outputs are not both at 0% duty but present a prefixed short pulse that is added to the effective duty cycle related to the audio signal.



The idea is to feed the power bridge with the minimum width pulses that keep the bridge just before the rise of the idle current; in this way a very small variation on a very low duty cycle can produce a correct low audio level at the output of the power bridge keeping the idle current close to zero.

The fractional PLL inside the FPGA allows the generation of a 400MHz high speed clock, which is enough to provide the extra room on the 192KHz PWM signals period needed by the offset pulse insertion without reducing the full range of the sample amplitude swing avoiding any clipping.

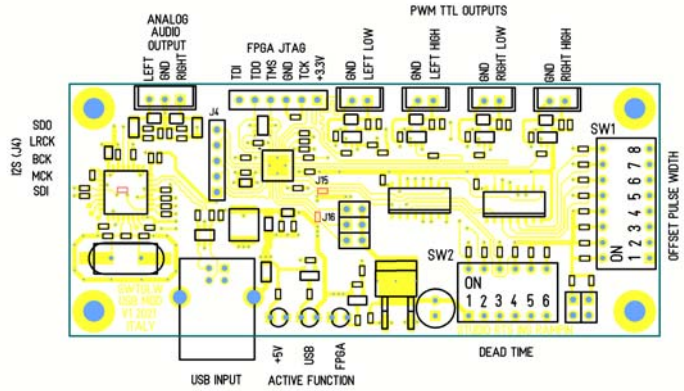
The width of the offset pulses T_{OFS} is selected by the dipswitch bank SW1, the dead-time between the PWM pulses T_{DT} is selected by SW2, both in steps of about 2.5 nsec.
On each dip-switch position #1 is the LSB; ON means logic 0, OFF means logic 1.

$$T_{OFS} = (N_{SW1}+1) \times 2.5 \text{ ns} \qquad T_{DT} = (N_{SW2}+1) \times 2.5 \text{ ns}$$

The sum $N_{SW1}+ N_{SW2}$ have to be less or equal to 35. If this sum is greater than 35, the PWM outputs go down because the overflow of the extra room allocated in the PWM signal period for the offset pulses.

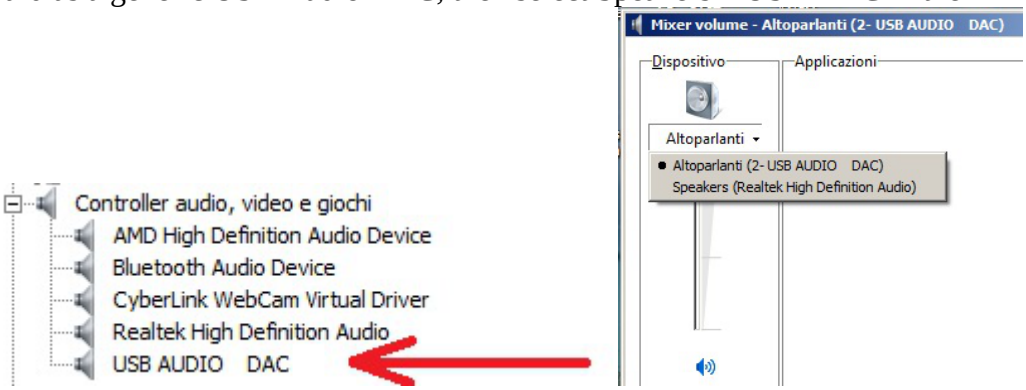
In order to properly operate the **SWITCHINGLOW POWER BRIDGE** it is necessary to select the minimum value of $N_{SW1}+ N_{SW2}$ that eliminates any audible residual white noise while listening to very low amplitude audio levels.

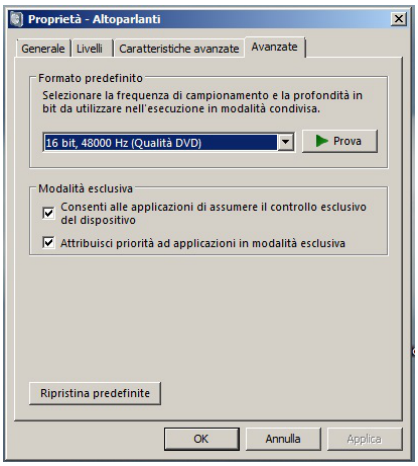
PWM pulse are provided as a couple of TTL level signals for each stereo channel (High Side Left, Low Side Left, High Side Right, Low Side Right).
The level of these outputs can be selected between 5V or 3.3V soldering respectly J16 or J15 on the bottom side of the PCB.
The outputs have a 150 ohm series resistor with a 100pF speed-up capacitor in parallel in order to drive directly the LEDs of any external optocoupler.
An 1.8Vpp on 32 ohm load analog audio output coming from the internal DAC of the PCM2706C is provide for test purpose.



The +5V LED indicator monitors the 5V power supply; the USB LED shows active audio samples presence, FPGA LED turns on after proper FPGA initialization.

Connect the **SWT-GLW USB MOD** to an USB port on a PC. The system have to recognize the board as a generic USB Audio DAC, then select Speakers – USB DAC in the Mixer Volume panel.





In Windows O.S. use Properties – Speakers - Advaced to select sample frequency 48KHz and 16 bit sample data width.
Operation with different sample rate / bit width is not guaranteed.

For further info please contact raites@studio-rts-ing-rampin.it
or visit www.switchinglow.com

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FCC / EMC Statement

The SWTGLW USB MOD electronic board is intended for evaluation only and does not require FCC Equipment Authorization (FCC Rule 2.803).
The SWTGLW USB MOD electronic board is designed to allow product developers to evaluate electronic components, circuitry or software associated with the board to determine whether to incorporate such items in their finished products.

The SWTGLW USB MOD is not a finished product and may not be resold, used as it is in or otherwise marketed as a final product unless all required FCC equipment authorizations or other countries EMC compliance certifications are first obtained.

“Operation is subject to the condition that this board not cause harmful interference to licensed radio stations and that this board accept harmful interference. Unless the board is designed to operate under part 15, 18 or 95 of this chapter, the operator of the board must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter” (Chapter I of Title 47, CFR).

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